(2)

AD-A196 961

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

UNIDIRECTIONAL MANCHESTER ENCODED
DATA TRANSFER VIA A FIBER OPTIC LINK

by

Robert Giles Ragsdale, Jr.

March 1988

Thesis Advisor: J.P. Powers

88

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
2a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution is unlimited
2b DECLASSIFICATION / DOWNGRADING SCHEDULE	
4 PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S)
6a NAME OF PERFORMING ORGANIZATION Naval Postgraduate School 6b OFFICE SYMBOL (If applicable) 62	7a NAME OF MONITORING ORGANIZATION Naval Postgraduate School
6c ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000	7b ADDRESS (City, State, and ZIP Code) Monterey, California 93943-5000
8a NAME OF FUNDING / SPONSORING ORGANIZATION 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c ADDRESS (City, State, and ZIP Code)	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO / PROJECT NO / TASK NO / WORK UNIT ACCESSION NO

11 TITLE (Include Security Classification)
UNIDIRECTIONAL MANCHESTER ENCODED DATA TRANSFER VIA A FIBER OPTIC LINK

12 PERSONAL AUTHOR(S)
RAGSDALE, Jr., Robert Giles

13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
Master's Thesis	FROM ____ TO ____	1988 March	

16 SUPPLEMENTARY NOTATION The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Manchester, Digital Data Transfer, Fiber Optic

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

The subject of this thesis is the application of Manchester encoding techniques to digital data transfer. Asynchronous receipt of digital data for decoding eliminates many of the technical implementation problems associated with synchronous transmission of data. The thesis goal was to construct the necessary hardware to allow Manchester encoded data transfer over a fiber optic data link. The scope of the project was limited to the transfer of byte size amounts of data from a microcomputer bus through the fiber link back to the computer bus. Successful coding, transmission, and decoding were accomplished as delineated in the hardware design section.

20 DISTRIBUTION / AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL John P. Powers	22b TELEPHONE (Include Area Code) 408-646-2082 22c OFFICE SYMBOL 62Po

DD FORM 1473, 84 MAR — 83 APR edition may be used until exhausted. All other editions are obsolete

SECURITY CLASSIFICATION OF THIS PAGE

U.S. Government Printing Office 1986—606-243

UNCLASSIFIED

Approved for public release; distribution is unlimited.

Unidirectional Manchester Encoded Data Transfer Via a Fiber Optic Link

by

Robert G. Ragsdale, Jr.
Lieutenant Commander, U.S. Navy
B.S., Virginia Polytechnic Institute,1972

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 1988

Author: Robert G. Ragsdale, Jr.
Robert G. Ragsdale, Jr.

Approved by: John P. Powers
John P. Powers, Thesis Advisor

Sherif Michael
Sherif Michael, Second Reader

John P. Powers
John P. Powers, Chairman
Department of Electrical and Computer Engineering

G E Schacher
Gordon E. Schacher,
Dean of Science and Engineering

ABSTRACT

The subject of this thesis is the application of Manchester encoding techniques to digital data transfer. Asynchronous receipt of digital data for decoding eliminates many of the technical implementation problems associated with synchronous transmission of data. The thesis goal was to construct the necessary hardware to allow Manchester encoded data transfer over a fiber optic data link. The scope of the project was limited to the transfer of byte size amounts of data from a microcomputer bus through the fiber link back to the computer bus. Successful coding, transmission, and decoding were accomplished as delineated in the hardware design section.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

TABLE OF SYMBOLS AND ABBREVIATIONS

AEN	Address Enable
BW	Bandwidth
BW-Dist	Bandwidth-Distance
C	Capacitor
Clad	Cladding
dB	Decibels
Dias	Diameters
EMP	Electromagnetic Pulse
Hz	Cycles Per Seconds (Hertz)
IOR	Input/Output Read
IOW	Input/Output Write
LED	Light Emitting Diode
μF	Microfarads
MM	Multimode
NRZ	Non Return to Zero
Ω	Ohms
P_e	Probability of Bit Error
R	Resistor
SM	Single Mode
SMA	Screw Type Fiber Optic Connector
SNR	Signal-to-Noise Ratio
ST	Bayonet Type Fiber Optic Connector
t	time
V	Volts

ACKNOWLEDGEMENT

My thanks to Professor John P. Powers for his assistance and patience during the course of this project.

I would also like to thank Mr. John Glenn for his irreplaceable technical support, knowledge, and limitless patience during the many hours that this design required. None of this would have been possible without them.

I. INTRODUCTION

The subject of this thesis is the application of Manchester encoding techniques to digital data transfer over fiber optic links.

Data transfer via the RS-232 interface has been the reliable standby for many years, but more recently the demand has been for faster transfer rates to ease the implementation of local area and extended networks .

Many techniques and schemes have been devised to allow this data transfer to take place more efficiently. One of the most significant problems associated with this goal has been decoding of the transmitted data. Basically, either the data must be received synchronously (i.e., requiring that the encoding clock frequency be available at the receiver) or it must be received asynchronously (i.e., without a clock reference).

Ultimately, though, some clock has to be used in order to successfully decode the data. One of the most successful methods has been to imbed the clock in the data stream with a Manchester encoding device and to remove the clock upon arrival at the decoder for use in synchronizing the decoding process. This thesis explores the implementation of this method of data transfer, with an imbedded clock, in fiber optic data links.

The goal of this thesis was to construct the necessary hardware to allow this asynchronous data transfer over the fiber optic link. This process, as noted in Figure 1, started in the IBM XT computer which was used as the host for the Manchester application. This circuitry was constructed on the second half of a JDR Microdevices prototype card with an address decode capability that is wired on the first halt. The memory location of the card was set to be Hex address 031C. This address, when applied on the address bus via the control logic, enabled the Manchester encode cycle. The Manchester chip encoded the data which the computer had placed on the data bus in synchronization with the address being placed on the address bus. The Manchester encoded data was transferred via the fiber optic link to the Manchester decode section of the same chip in a loop-back design which minimized the required equipment, i.e., only one computer and prototype card was required. The block diagram of Fig. 1.1shows the graphical description of the concept. After decode, the data was accessible to the host data bus. A detailed explanation of these operations is located in Chapter IV.

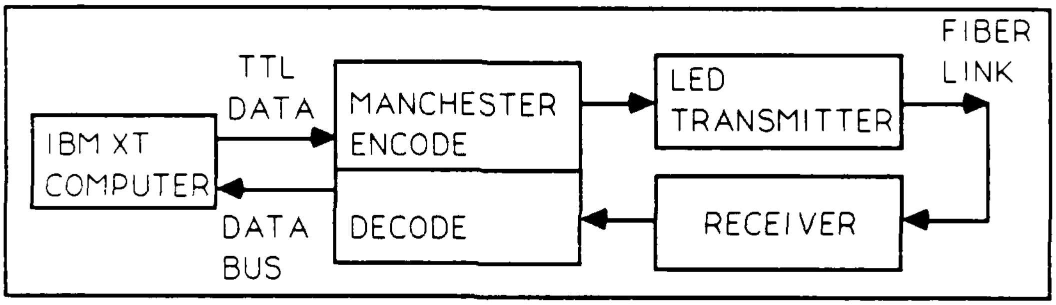

Figure 1.1- Ceneral Block Diagram

In order to limit the scope of the project, the goal was to successfully encode, transfer, and decode byte size amounts of data. This was accomplished as indicated in the last part of Chapter IV on the hardware design.

To briefly outline the course of this development, first a knowledge baseline will be established by describing in Chapter II the background involved in fiber optic link design and a discussion, in general, of the theory of the Manchester coding format. Chapter III explains in detail how Manchester encoding and decoding is implemented, generically, in the chip chosen for this application. From this solid base of knowledge, the hardware design is implemented Chapter IV. Chapter V completes this thesis with conclusions and recommendations for further development of this particular concept.

II. BACKGROUND

A. FIBER OPTIC DATA LINK

1. Description

The advantages of a fiber optic link are legion. Advantages of particular interest to the military over twisted wire pair transmission are reduced weight, increased degree of difficulty in intercepting the transmitted intelligence, no potential for arcing (allowing fiber to be laid through flammable liquids tanks, etc.), more bandwidth, and relative invulnerability to electromagnetic pulse, EMP.

The primary components of the fiber optic data link consist of the transmitter section, the receiver section, and the optical fiber linking these two. The link may be unidirectional or, more usefully, bidirectional with either a microprocessor controlling the link transmission direction or a wave-division-multiplexed full duplex coupler, using two different wavelengths of source light, laser or LED, transmitted simultaneously in opposite directions. Each unit contains a source and a detector and a dichroic filter to allow the duplex operation.

An example of this type of coupler is ADC's Bidirectional Connectorized Active Full Duplex Coupler, model CAF. This coupler operates at nominal wavelengths of 730 and 865 nanometers. The transmit and receive signals, operating at different wavelengths, are separated by the use of the CAF's internal reflective surface and specially designed optical coatings that result in excellent optical isolation. [Ref. 1]

Many interrelated factors drive the selection of the components required to construct a functional fiber optic data link. Cost, link capacity (bandwidth), projected link lifetime and reliability, type of source (LED or laser), type of detector, and number of stations sharing the link are just a few of these variables.

2. Optical Fiber

After deciding on the maximum potential bandwidth required for the particular fiber optic link application, the physical attributes (and cost range) of the fiber can then be determined.

TABLE 2.1- PHYSICAL SPECIFICATIONS OF TYPICAL FIBERS

Type	Core /Clad. Dias.(um)	BW-Dist. Product	Application
1-SM	8/125	5000 MHz-km high data rate	long distance
2-MM	50/125	500 MHz-km and data rate	med. distance
3-MM	62.5/125	100 MHz-km	local area net
4-MM	100/140	50 MHz-km med. data rate	short distance
5-MM	200/600	50 MHz-km	local area net

As can be seen from Table 2.1, the first type, a single mode fiber with an 8 micrometer core and 125 micrometer cladding diameter (commonly written as 8/125) constructed from silica materials of varying indices of refraction, has the largest bandwidth-distance product. Due to reduction in production costs, lower attenuation losses, and other factors, this particular variety of fiber is tending to replace the more expensive multimode fibers. Regardless, both of these fibers are less costly than the equivalent wire choice for the same data rate (if wire could match the data rate).

At the other end of the cost spectrum lies the fifth type of multimode fiber. It consists of a relatively large core and cladding combination which may be constructed from plastics, of differing index of refraction, or silica based material. Due to the size and material composition, the power losses per kilometer tend to be quite a bit larger than the preceding four examples. This type of fiber, as indicated, would make a good choice for a low data rate, short distance net.

3. Transmitter

Consistent with the design goal of this project was the choice of an efficient, compatible fiber optic transmitter/receiver set. After study and analysis, it was found that the Hewlett Packard HFBR-0400 series of components most readily lent themselves to successful design implementation. First, a more detailed look at the transmitter specifications will be undertaken.

The HFBR-1402 Standard Transmitter was chosen to implement the design. Distances to 2.5 kilometers at data rates up to 5 MBd are achievable using the HFBR 1402/1404 transmitter and the HFBR-2402 receiver [Ref. 2] . The transmitter contains an 820 nm GaAlAs LED with a power budget and coupling efficiency sufficient to allow coupling into a number of different fiber sizes, from 50/125 um to 100/140 um and 200 um PCS, and into a variety of local area network configurations, i.e., STARLAN, Token Ring, etc. The physical housing supports the use of an industry standard SMA connector for the fiber portion of the link. The literature indicates a typical rise/fall time of 4.0 nanoseconds and a worse case propagation delay (from LOW to HIGH) of 10.0 nanoseconds.

Both of these measurements are at a forward input current of 60 milliamps, the maximum rating for the transmitter drive current.

4. Receiver

As would be expected, the design of the receiver housing is very similar to the transmitter, supporting the same SMA standard connector, allowing use of the same range of fiber sizes as indicated in the transmitter section immediately above. The heart of the receiver, the photodetector, is a monolithic photo-IC containing a photodetector and a dc amplifier. With the associated open collector Schottky transistor on the IC, the receiver is compatible with both TTL and CMOS logic. The following table, Table 2.2, is taken in part from Ref. 2 and delineates the dynamic characteristics of the receiver.

TABLE 2.2- DYNAMIC CHARACTERISTICS OF THE HFBR-2402 RECEIVER (FROM REF. 2)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Peak Input Power	P_{rh}	-	-	-40.0	dBm	
Level Logic HIGH		-	-	0.1	uW	Ip = 820 nm
Peak Input Power	P_{rl}	-25.4	-	-11.2	dBm	T_a = +25 C
Level Logic LOW		2.9	-	76.0	uW	IOL = 8 mA
		-24.0	-	-12.0	dBm	-49< TA < 85 C
		4.0	-	63.0	uW	IOL = 8 mA
Propagation Delay	T_{plhr}	-	65.0	-	nsec	T_a = +25 C
LOW to HIGH		-	-	-		P_r = -21 dBm
		-	-	-		DR = 5 MBd
		-	-	-		BER = 10-9
Propagation Delay	T_{plhr}	-	49.0	-	nsec	
HIGH to LOW						

B. MANCHESTER CODING

As indicated before, there exists a number of code formats which are used in the various types of applications. Figure 2.1 shows a selection of coding format waveforms for comparison purposes. Among the formats are non-return-to zero (NRZ) and return-to-zero (RZ) unipolar, bipolar, and a biphase pulse code format. For fiber optic data transmission, the biphase format is a coding format of choice.

A mid data bit transition is the distinguishing characteristic of Biphase coding. This transition is negative-to-positive for zero and positive-to-negative for one. This is succinctly stated in Ref. 3 as follows:

> This biphase-level shift format has succeeded in eliminating all the DC components, at the expense however, of increasing the transmission bandwidth when transmitting the same amount of data.

Because of the bandwidth available with a fiber optic data link, this *requirement* for increased bandwidh is a problem of no particular significance.

As there is a transition during every bit cycle (matching the encoding clock frequency), the encoding clock can be recovered in the decoding circuitry allowing for asynchronous receipt of data at a choice of clock frequencies greatly exceeding (by magnitudes) those available with the RS-232 interface. This simplifies link design for systems which are physically separated by long distances.

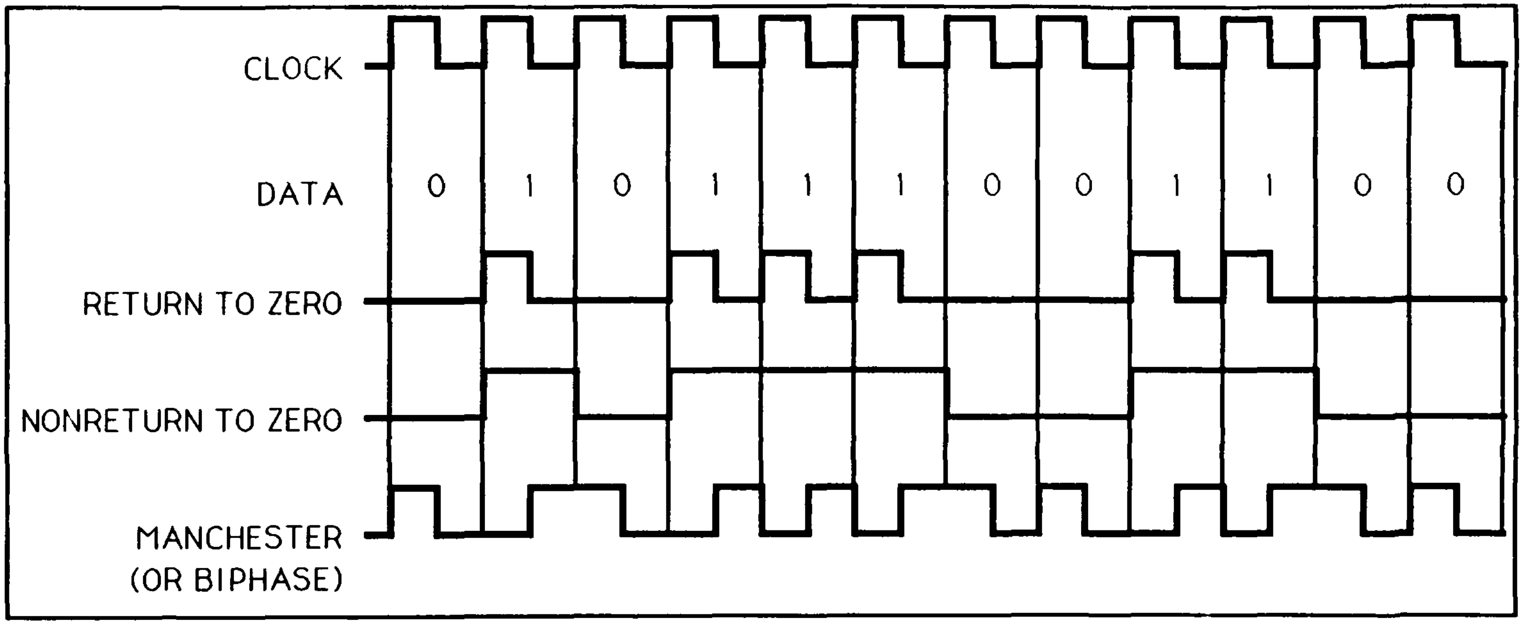

Figure 2.1- Waveforms Of Various Coding Formats [Ref. 3]

III. MANCHESTER THEORY OF OPERATION

Since the Manchester encoding process is the center of this application, this section will deal with a detailed description of the encoding and decoding process as accomplished by the IC chip.

A. ENCODING PROCESS

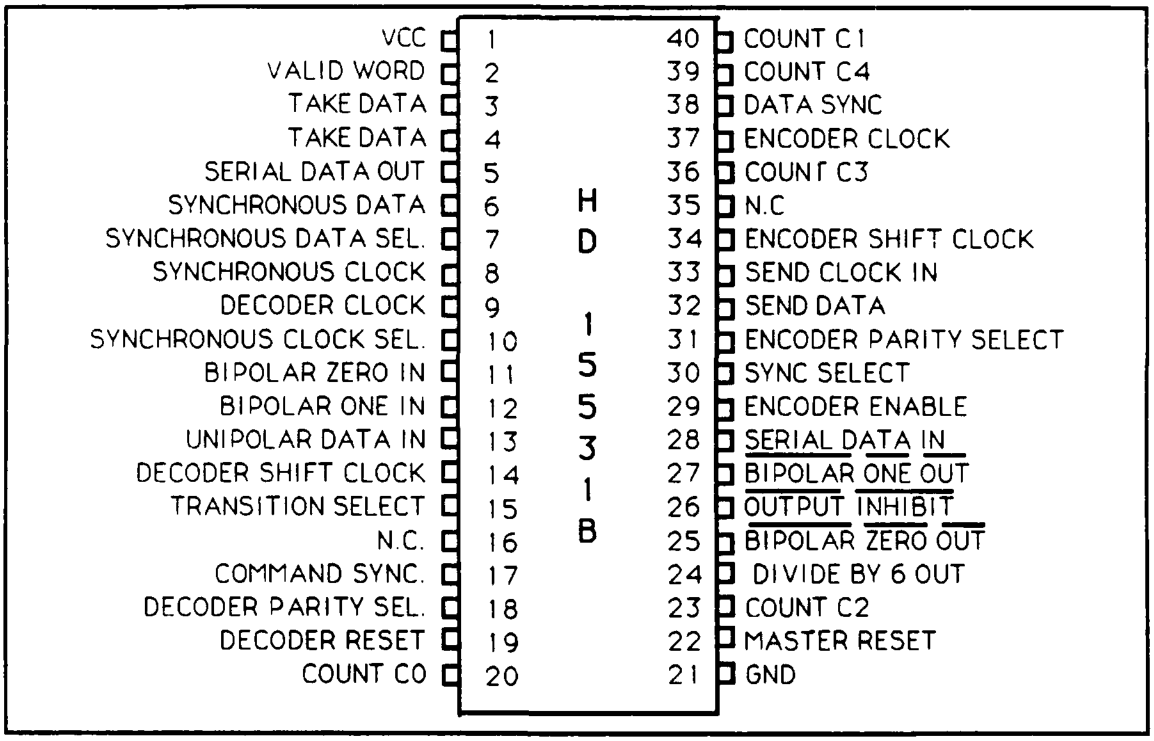

Figure 3.1- Harris Manchester Chip, HD-15531-B [Ref. 4]

An investigation of the alternatives in the field of Manchester encoding-decoding devices was conducted. The chip of choice for this application was the Harris Corporation's HD-15531B CMOS Programmable Manchester Encoder-Decoder.

This section presents a description of this encoding process in detail. Figure 3.1 shows the pin-out of the Harris chip and may be used for reference during the Encoder-Decoder discussion.

Figure 3.2 on the next page shows the timing and the pictorial representation of the clock and control signals that pertain in the following explanation of the encoding sequence for a data byte.

One of the significant advantages of this particular chip is the freedom to select the data byte size to correspond with the system being used without having to buy a new chip for each new system. The following table, from Ref. 4, is a partial listing of the required values for programming (pin wiring) the data length:

TABLE 3.1- FRAME COUNT FOR PROGRAMMING THE HARRIS MANCHESTER CHIP

FRAME DATA BITS	LENGTH (BIT PERIODS)	PIN WORD C4	C3	C2	C1	C0
2	6	L	L	H	L	H
3	7	L	L	H	H	L
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
–	–	–	–	–	–	–
28	32	H	H	H	H	H

Because of the eight bit data bus size of the computer, a Frame Data Bit size of eight was chosen in order to encode the data in whole bytes.

The Encoder clock, applied at the Send Clock input, needs to run at a speed of at least double the data rate, i.e., it can be more than the double the data rate. Send Clock was produced by using the divide-by-six circuit provided on the

Manchester chip to countdown the Encoder Clock. For this application the clock speed was not critical.This was due to the fact that the data was transferred one byte at a time with a comparatively long time (relative to computer speeds) between bytes. The Manchester portion of the application used a 20 MHz clock crystal while the JDR address decode portion used the host computer clock of 4.77 MHz.

Since the data was byte size, the eight data bits equated to a Manchester frame length of twelve as indicated in Table 3.1. Odd parity was selected for both the encoder and decoder of the Manchester via DIP switches, set high, located on the application board. Even parities could have been selected by setting the same switches low.

Since the concept itself was being tested, instead of picking a particular data rate, a 20 MHz clock crystal was installed on the application board. This allowed coverage of a full range of potential data rates for both the Encoder and the Decoder, up through 10 MHz, well past the clock speed for the computer used. The test bed computer was an IBM XT clone purchased through Jameco Electronics of Belmont, California. The following is from Ref. 4 describing the Encode cycle:

> The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of the ENCODER SHIFT CLOCK. This cycle lasts for one word length or K+4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a COMMAND SYNC or a low will produce a DATA SYNC for that word. When the Encoder is ready to accept the data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods. During these K periods, the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK. After the sync and Manchester II encoded data are transmitted through the BIPOLAR ONE (not) and BIPOLAR ZERO(not) outputs, the Encoder adds on an additional bit which is the parity for that word. At any time a low on OUTPUT

INHIBIT(not) input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

A high applied to the Master Reset will cause the encoder to abort a data transmission. A low-to-high transition of Send Clock during or after the high will cause the reinitialization of the Encoder and clearing of the internal counters. [Ref. 4]

Figure 3.2 shows the relationships between several of the previously mentioned signals. The Encoder Shift Clock is counted down from the Send Clock by half. The Encoder Enable comes from the LS138, Figure 4.1, after address decode. The next signal, Sync Select, indicates that a Command vice a Data Word is being currently encoded for transmission. Send Data is a chip output signal to indicate that the chip is prepared to encode the data and is a result of the previous high at Encoder Enable. The next to the last signal is the data being clocked into Serial Data In of the Manchester Chip. The last signal is the encoded Manchester data frame output from the chip for transmission through the fiber optic link.

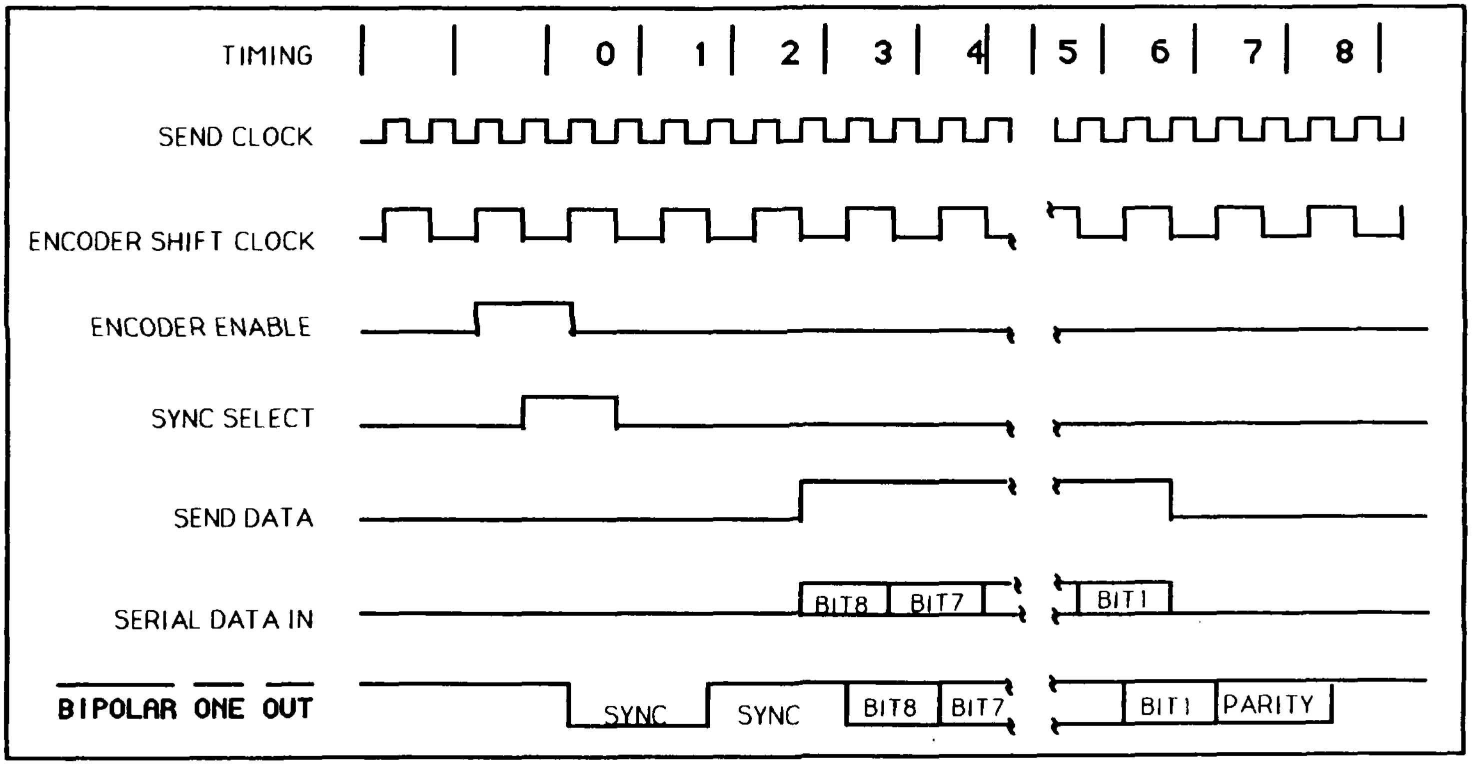

Figure 3.2- Encoder Timing Diagram [Ref . 4]

B. DECODING PROCESS

As indicated previously, one of the key requirements for the decoding circuit is to be able to operate asynchronously to ease the problems of circuit design. This was also accomplished by use of the Harris Manchester chip.

An excellent description of the two options for decoder operation is taken from Ref. 4 as follows:

> To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS DATA input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data, (e.g. from BIPOLAR ONE OUT(not) on an Encoder).

A Harris applications engineer indicated that, contrary to the Harris Manchester literature, BIPOLAR ONE OUT(not) was inverted and then returned to the UNIPOLAR DATA input of the decoder. For the application, this inversion was accomplished prior to being transmitted through the fiber optic link. The Decoder operation was very succinctly described in the Harris Manchester data sheet as follows:

> The Decoder is free running and continuously monitors its data input for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized, the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high and remain high for K SHIFT CLOCK periods. where K is the number of bits to be received. If the sync character was a data sync, the DATA SYNC output will go high. The TAKE DATA output will go high and remain high while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT

CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock.

After all the bits have been read out from the Manchester chip, the signal Valid Word goes high if there were no Manchester bit errors or no parity errors. Here again, Parity is selectable, with high parity being selected with a high to the Decoder Parity Select pin or a low to the same pin for low parity. [Ref. 4]

Taking a more indepth look at some of the signals described in the decoder operation note the next figure, Figure 3.3. Ignoring the top signal, SYNCHRONOUS CLOCK because the application uses asynchronous operation, the next signal is the DECODER SHIFT CLOCK. This clock shifts the decoded data from the Manchester to the LS164 serial-to-parallel shift register. The input data stream, from BIPOLAR ONE OUT (not) through the fiber optic link, is presented to the UNIPOLAR DATA IN pin as represented in the third signal. The fourth signal, TAKE DATA, is raised after the decoder receives the SYNC plus two valid Manchester bits. SERIAL DATA OUT represents the decoded output data stream being clocked to the LS164. The last signal, VALID WORD, is raised after the last encoded bit is processed with no Manchester bit or parity errors.

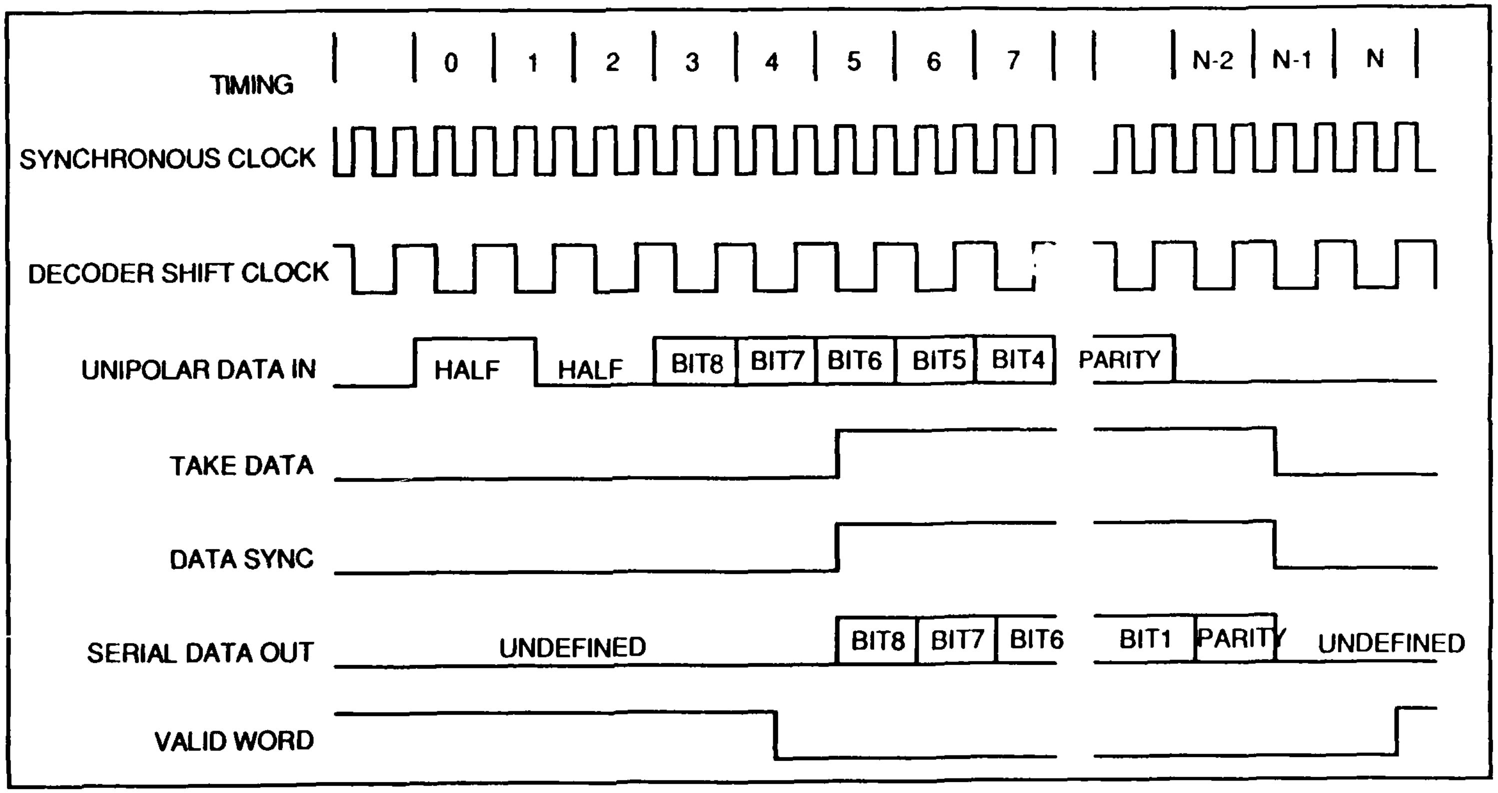

Figure 3.3- Manchester Decoder Timing Diagram [Ref. 4]

IV. DETAILED HARDWARE DESIGN

A. MANCHESTER CHIP SELECTION VIA ADDRESS DECODING LOGIC

To use one of the expansion slots in the IBM XT computer for the data transfer application, it was necessary to be able to "locate" the JDR prototype card with the associated Manchester application in the expansion slot, within the computer memory, to be able to communicate with it.

This necessitated the use of address decoding logic so that a particular address, when placed on the address bus by the host computer, would cause the selection of the Manchester application. The most easily implemented decoding was a JDR Microdevices PR-1 prototype card which addressed the block of memory, Hex 300-31F, in eight groups of four consecutive addresses each. The address decode logic, as indicated in Figure 4.1, forced a low from pin 7 (Select 7) of the LS138 when the address chosen for the JDR card/Manchester application, Hex 031C, was placed on the address bus. The 74LS85 and the 74LS138 are the main chips in the decoding scheme. The 74LS244's enable pins are held low by being tied to ground. The 74LS244's are line drivers capable of handling eight bits at a time. Because the enable pins are active low and are tied to ground, these chips pass the bus signals that they buffer through [Ref. 5]. In the first stage of the decoding process, addresses A5-A8 are compared in the 74LS85 (a comparator chip), as indicated in Figure 4.1, with pins 9, 12, 13, and 1 wired respectively to values of 1, 0, 0, and 0. When that portion of the decoding is passed correctly, a high signal on pin 6 is combined with the indicated additional logic involving AEN, IOR, and IOW to generate the final of three enables for the 74LS138 (3-line to 8-line decoder/demultiplexer).

The AEN, IOR, IOW pins and the 74LS85 pin 6 value are also used in the selection logic to enable the 74LS245 octal bus transceiver (which interfaces the data bus in the computer and the data bus on the JDR board) and to choose the direction of the data transmission in the 74LS245 from data bus to Manchester or Manchester to data bus.

The other enables for the 74LS138 are tied high or low to +5V or ground as required to be constantly enabled. Address lines, A2-A4, are used in the final step of decoding in the LS138 to differentiate between the Select 0 to Select 7 outputs, each of which addresses the previously mentioned block of four consecutive addresses.

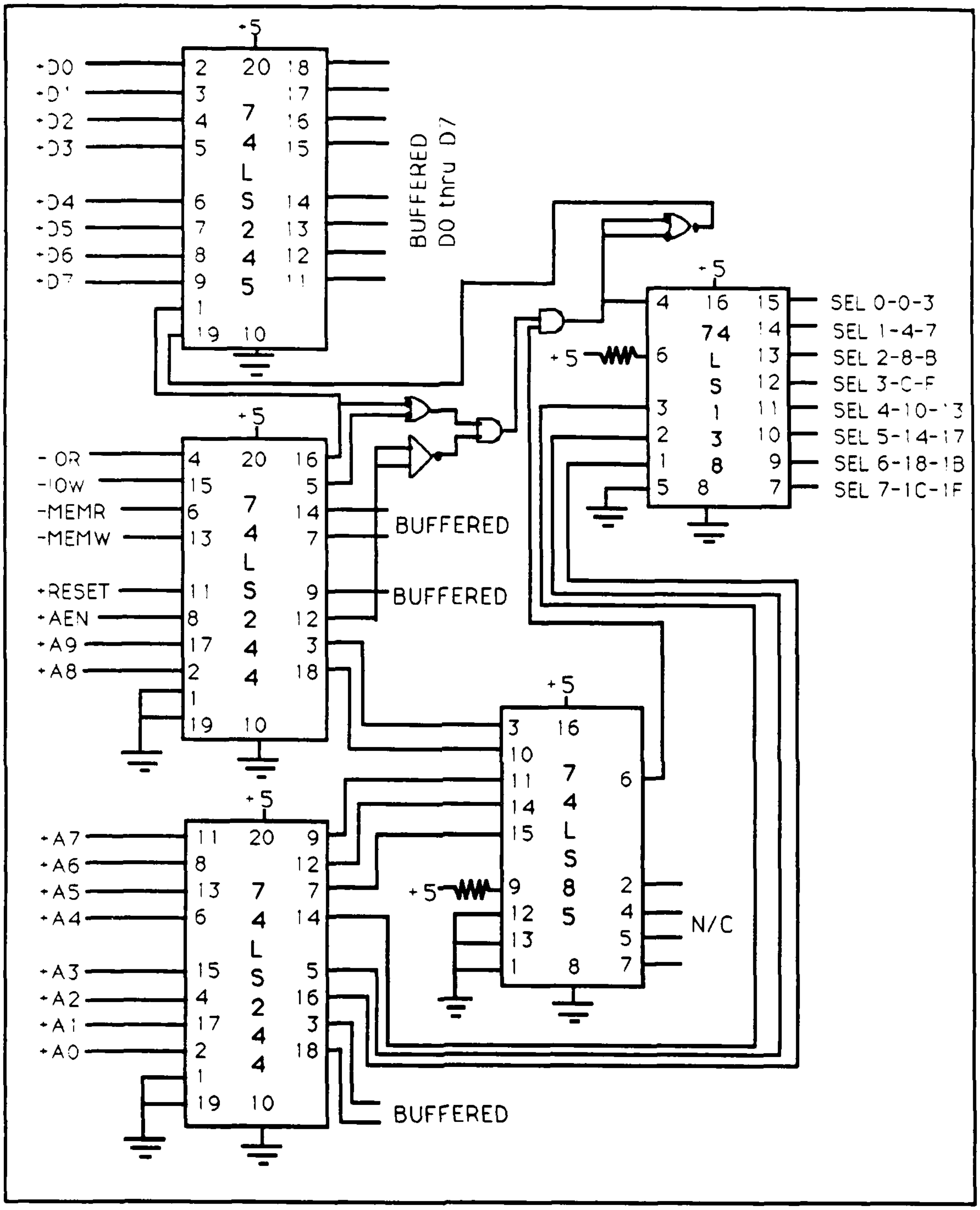

Figure 4.1- Manchester Chip Selection Via Address De code [Ref. 5]

B. ENCODING-DECODING SECTION

As discussed before, address 31C causes the JDR decode logic to select pin 7 of the LS138 (a low). This select goes directly to the SH/LD(not) of the LS 165 (parallel load 8-bit shift register), causing it to load the current value of the data lines into A through H of the LS165. Also at this point, Select 7 is applied to the two inputs of a two input NAND gate. This inverted signal is sent to pin 29, Encoder Enable, of the Manchester chip.

Several clock cycles later, the Manchester is ready to input data and raises the signal, Send Data (pin 32). This signal plus the Encoder Shift Clock (pin 34) are sent to the two inputs of a two input NAND gate. This causes the encoder Shift Clock to be sent to the clock input of the LS165 during the time Send Data is high for the purpose of shifting the data in A-H out QH (pin 9) of the LS165 to Serial Data In (pin 28) of the Manchester. This will occur because the timing is such that Select 7 is now back to a high. A high on the SH/LD(not) pin of the LS165 allows the shift process to take place.

After internal processing in the Manchester, the data frame, consisting of the original data bits preceded by two synchronization pulses and trailed by a parity bit, is ported out of the Manchester via Bipolar One Out(not) (pin 27). This output is then inverted with a NAND gate and goes to the TTL input of the circuit as shown in Figure 4.3.

The received signal, at the other end of the fiber optic link, proceeds from pin 6 of the HFBR-2402 as indicated in Figure 4.4. The signal is inverted with a two input NAND gate as shown in the same figure and is then wired into Unipolar Data In (pin 13) of the Manchester. This is the TTL input to the decoder. The circuitry of the Manchester chip monitors continuously for a sync signal plus two valid Manchester bits to start the output cycle. When the data sync is received, Data Sync (pin 38) goes high during the output of decoded data. Take Data (pin 4) also goes high for the duration of the output of decoded data through Serial Data Out (pin 5).

For this application, Take Data and the Decoder Shift Clock were the two inputs to a two NAND gate, the output of which provided the clock for the LS164 (serial-to-parallel shift register) to shift the decoded data from the serial port of the Manchester into the register.

The SERIAL DATA OUT (pin 5) was wired to A and B (pins 1 and 2) of the LS164. VALID WORD was wired directly into pin 11 of the LS374. With VALID WORD low, the D inputs of the LS374 followed the values on the data pins of the LS164 as the serial data was clocked in from the Manchester chip. One clock cycle after the last bit of data was shifted into the LS164, VALID WORD (pin 2) went high. This high caused the LS374 Q outputs to be latched at the values then resident on the D input pins, making these values available to the host computer data bus. Figure 4.2 shows this circuit wiring. .

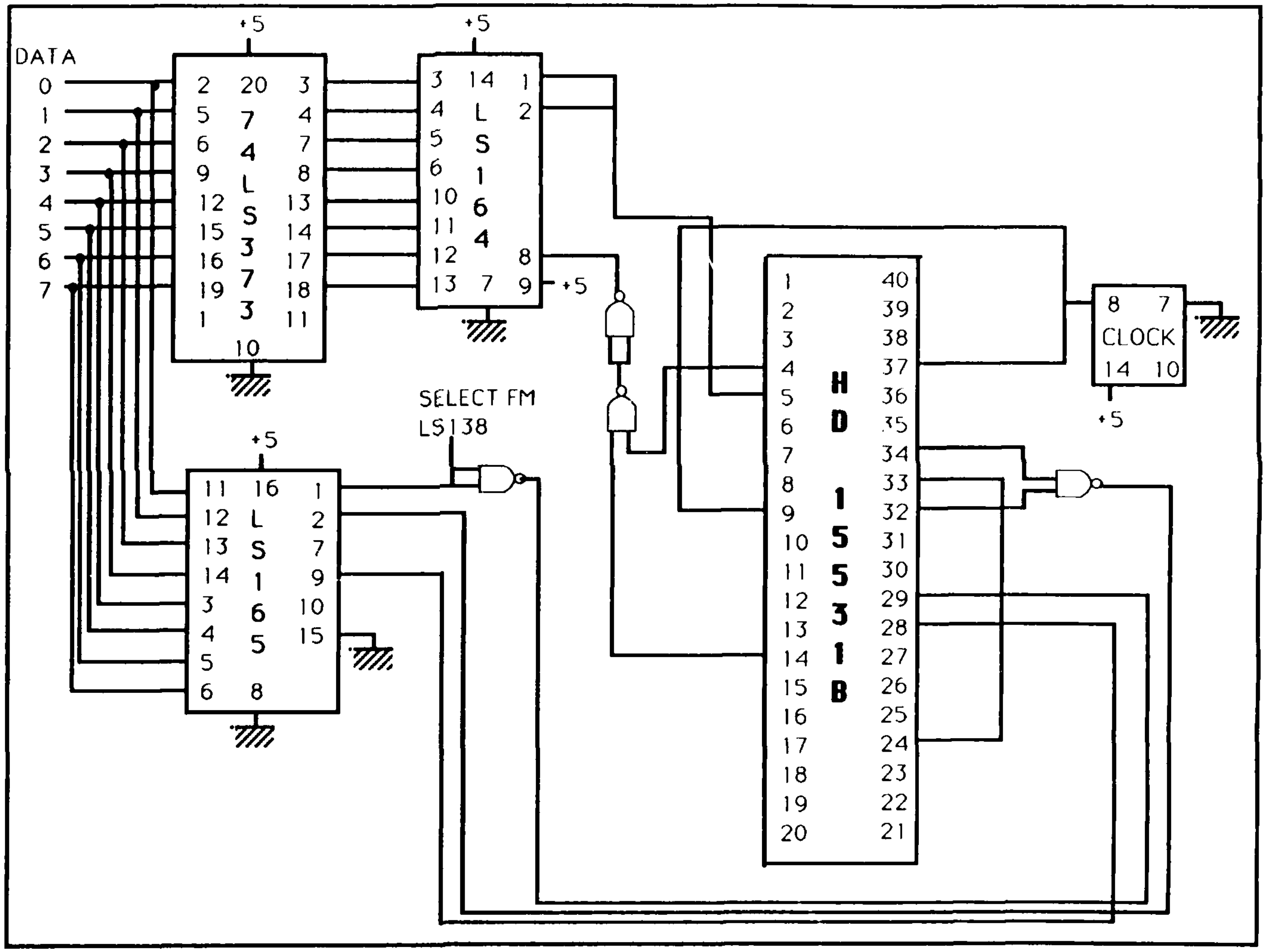

Figure 4.2- Manchester Data Transfer Application Circuit

C. FIBER OPTIC DATA LINK

The easiest implementation of the fiber optic data link was to use the suggested driver and receive circuit from Ref. 2 as shown in Figures 4.3 and 4.4, respectively. The operation of this link has a maximum transmission rate of five megabaud which will more than adequately meet the requirements of a fiber optic data link.

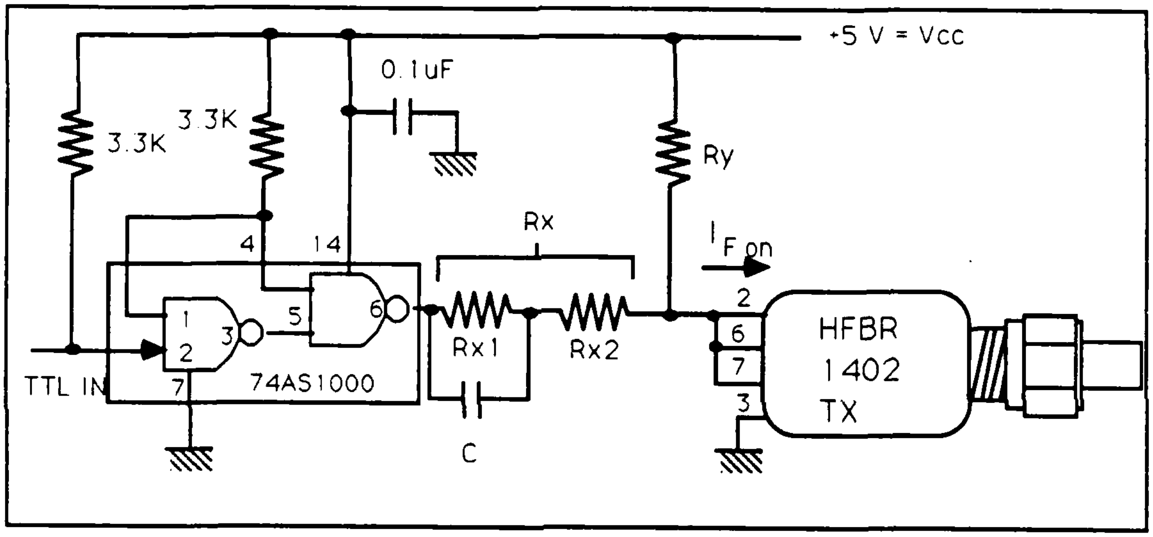

Figure 4.3 - HFBR 1402 Transmitter [Ref. 2]

The 74AS1000 serves as a quadruple two-input positive NAND buffer/driver for the transmitter circuitry. Looking at the drive circuit in Figure 4.3, the literature suggests using a pre-bias current to reduce the junction capacitance and a "speed up" capacitor, denoted as C in the figure, to reduce the rise and fall times. The transmitter power out is a direct function of the transmitter drive current, I_F. The other variable values in the figure, R_y, R_x, R_{x1}, R_{x2}, and C, can be determined from the following equations [Ref. 2] once the desired power out, i.e., drive current, has been decided.

$V_F = .312\,(I_F) + 1.55$ 1.1

(The equation for V_F is an approximation fitted from data given in Figure 2 of Ref. 2)

$R_Y = \{(V_{CC} - V_F) + 3.2\,(V_{CC} - V_F - 1\,.4V)\} / I_{FON}$ 1.2

$R_X = \{(R_Y / 32) - 10\,W \}$ 1.3

$R_{X1} = (R_X - 10\,W)$ 1.4

$R_{X2} = R_{X1} - 10$ 1.5

$C = 2.0\ \text{nsec} / R_{X1}$ 1.6

The application used 27 milliamps for the forward current. This corresponded to a V_F of 1.7 volts. Having used the equations listed above, the results were as follows:

R_Y = 348 ohms R_{X1} = 54.4 ohms

R_X = 98.8 ohms R_{X2} = 44.4 ohms

C = 36.8 picofarads

These calculated values were rounded off to the following "off the shelf" values:

R_Y = 330 ohms R_{X1} = 55 ohms

C = 38 picofarads R_{X2} = 47 ohms

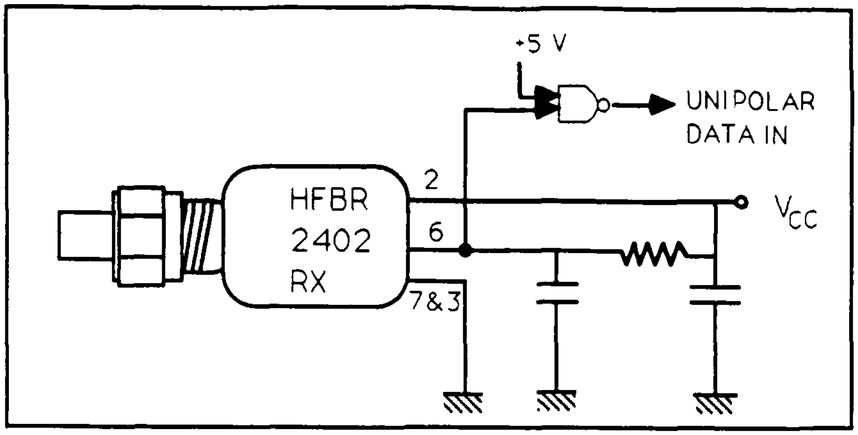

Figure 4.4 -HFBR-2402 Receiver Circuit [Ref. 2]

The receiver circuit is an easy to construct design as seen in Figure 4.4. The following from Ref. 2 describes the HFBR-2402 Receiver:

> The HFBR-2402 Receiver incorporates an integrated photo-IC containing a photodetector and dc amplifier driving an open-collector Schottky output transistor. The HFBR-2402 is designed for direct interfacing to popular logic families.

Detailed, additional information on the characteristics, both electrical and dynamic, may be found in Section 2, part A in the discussion of the fiber optic data link.

D. EVALUATION

The design goal for this hardware application was to be able to transfer data from the computer through the address decode circuitry, the Manchester encoding, the fiber optic link, the Manchester decode circuitry, and to have the original data return back to the data bus.

Testing of this function was accomplished with the following short program which put an arbitrary piece of data on the data bus in conjunction with the designed for address of Hex 031C.

TABLE 4.1 - DATA TRANSFER TEST PROGRAM

0100	MOV	DX, 031C	Load Hex 031C into data register
0103	MOV	AL, 41	Load 41 into lower half address register
0105	OUT	DX, AL	Move data in AL out of port in DX
0106	MOV	DX, 0318	Move 0318 to data register
0109	NOP		
010A	NOP		
010B	IN	AL, DX	Input value at DX to lower half address register
010C	NOP		
010D	JMP	0100	Jump to memory location 0100 and continue

The address, Hex 031C was loaded into DX. The data bytes, Hex 41, were loaded into AL. The two of these were then put on the respective buses with the OUT command. The circuit board received the data, encoded it, transmitted it through the fiber optic link, decoded it and presented the data to the bus. After a short timing pause, the data/address buses were read and the associated data recovered. The program was then looped back to the beginning, 0100.

Initially, the program was run in the trace mode to investigate the overall accurate functioning. After this was determined to be correct, the program was run at the computer clock speeds in the designed loop-back scheme. The data was again found to be correctly located on the output pins of the 74LS374, the interface between the computer data bus and the circuit data bus.

Figure 4.5 shows a selection of the Manchester control and clock signals of particular interest noted during this process. These signals were captured with a Hewlett Packard 1615A Logic Analyzer and then transcribed to paper with a Hewlett Packard 7470A Plotter. As can be seen from the figure, the control signals timing for the constructed circuit matches the timing indicated by the earlier section on the Manchester Encoder-Decoder as expected.

A little more detail on this particular figure follows. The first signal is the selection from the LS138. This signal goes to the ENCODER ENABLE of the Manchester. The third signal is SEND DATA returned from the Manchester, several clock cycles later, when the chip is ready to encode data. This signal combined with the ENCODER SHIFT CLOCK in the NAND gate produces the fifth signal, the LS165 CLOCK, which can be seen to exist only for the duration of SEND DATA. Next, the LS165 QH signal shows the data being shifted from QH, Serial Data Out of the LS165 chip, to SERIAL DATA IN (Pin 28) of the Manchester. The next to the last signal is serial data coming from SERIAL DATA OUT of the Manchester decode circuit after being transmitted through the fiber optic link. The very last signal, VALID WORD, demonstrates the chip's response, the signal goes high, to the successful decode of the data byte without any parity or Manchester errors.

V. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The circuit as designed and constructed functioned as desired. The design goal of limited data transfer with Manchester encoding-decoding techniques to test the functionality of the concept was verified.

The Digital Logic Analyzer would not properly reproduce the data transfer in the Timing Diagram mode, although it did show the data transferred in the List Mode. In order to verify the data transfer, Table 5.1 is a partial reproduction of a screen print from the IBM XT computer while running IBM Debug in the trace mode from DOS.

TABLE 5.1- IBM XT COMPUTER SCREEN PRINT

```
AX = 0041     BX = 0000   CX = 00FF   DX = 0318
DS = 2CE0     ES = 2CE0   SS = 2CE0   CS = 2CE0   IP = 0100
2CE0 : 0100   BA1C03                  MOV         DX, 031C

AX = 0041     BX = 0000   CX = 00FF   DX = 031C
DS = 2CE0     ES = 2CE0   SS = 2CE0   CS = 2CE0   IP = 0103
2CE0 : 0103   B041                    MOV         AL, 41

AX = 0041     BX = 0000   CX = 00FF   DX = 031C
DS = 2CE0     ES = 2CE0   SS = 2CE0   CS = 2CE0   IP = 0105
2CE0 : 0105   EE                      OUT         DX, AL

AX = 0041     BX = 0000   CX = 00FF   DX = 031C
DS = 2CE0     ES = 2CE0   SS = 2CE0   CS = 2CE0   IP = 0106
2CE0 : 0106   BA1803                  MOV         DX, 0318
```

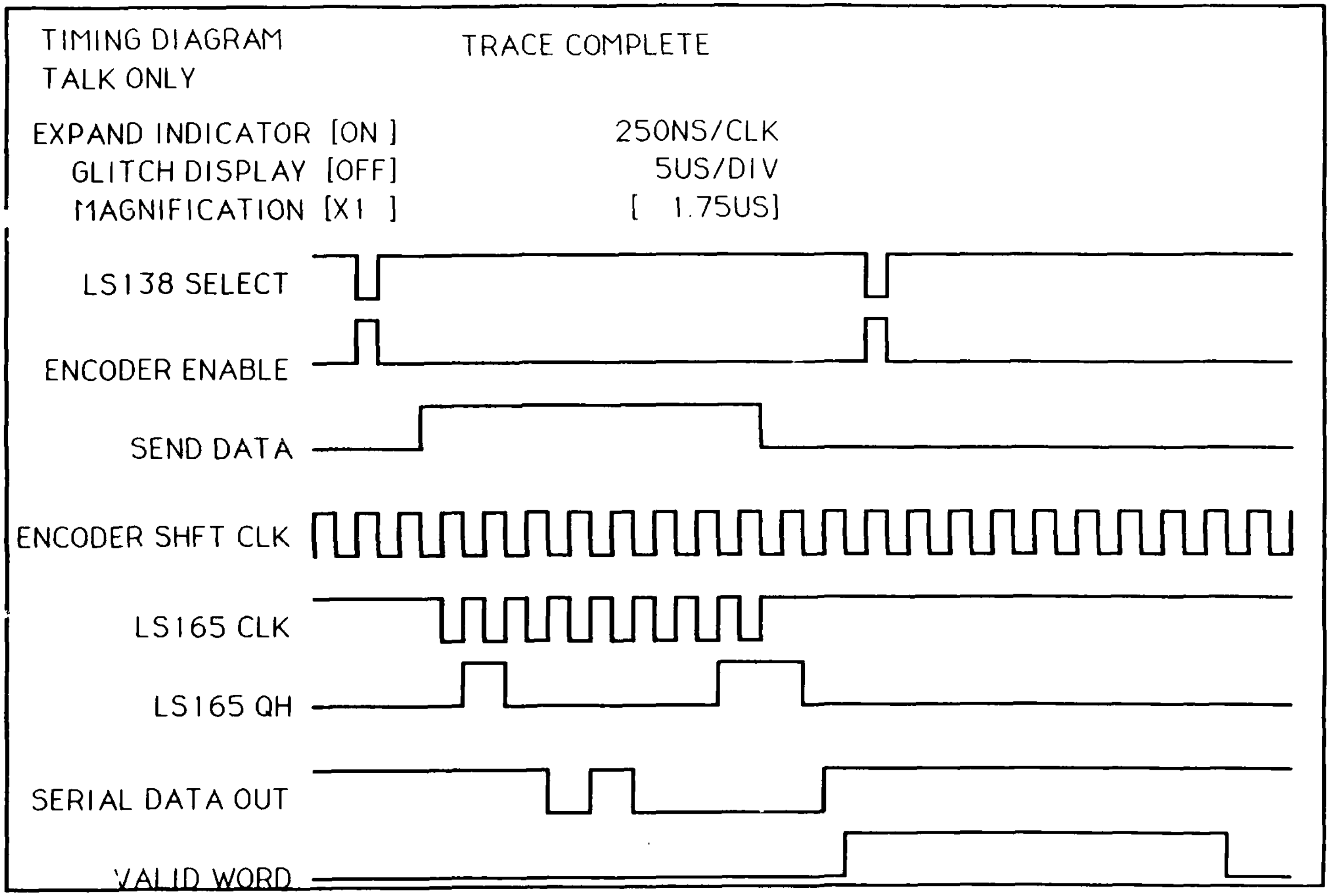

Figure 4.5- Timing of Control Signals and Selected Clocks

```
AX = 0041    BX = 0000    CX = 00FF    DX = 0318
DS = 2CE0    ES = 2CE0    SS = 2CE0    CS = 2CE0   IP = 0109
2CE0 : 0109  90                        NOP

AX = 0041    BX = 0000    CX = 00FF    DX = 0318
DS = 2CE0    ES = 2CE0    SS = 2CE0    CS = 2CE0   IP = 010A
2CE0 : 010A  90                        NOP

AX = 0041    BX = 0000    CX = 00FF    DX = 0318
DS = 2CE0    ES = 2CE0    SS = 2CE0    CS = 2CE0   IP = 010B
2CE0 : 010B  EC                        IN          AL, DX

AX = 0041    BX = 0000    CX = 00FF    DX = 0318
DS = 2CE0    ES = 2CE0    SS = 2CE0    CS = 2CE0   IP = 010C
2CE0 : 010C  90                        NOP

AX = 0041    BX = 0000    CX = 00FF    DX = 0318
DS = 2CE0    ES = 2CE0    SS = 2CE0    CS = 2CE0   IP = 010D
2CE0 : 010D  EBF1                      JMP         0100
```

This test program is documented in TABLE 4.1. In brief, AX is the register where the data to be transferred is located. The command "OUT DX, AL" (in the third group of Table 5.1) causes the data to be applied to the data bus while the Manchester selecting address is placed on the address bus. Four program steps later, the command "IN AL, DX" (in the seventh group of Table 5.1) causes the host computer to read the data then present on the bus. In every case, the target data was on the bus after being completely processed through the Manchester circuit as indicated by the AX = 0041 items. The other registers in the table printout are associated with the trace mode operation, but are not relevant to this discussion.

This was by no means a rigorous or all-encompassing evaluation of the hardware capabilities and limits. It does provide a starting point to launch additional research to attain the end goal of constructing and evaluating a high speed fiber optic data link with time division multiplexed (and or wave division multiplexed) bidirectional capabilities.

B. RECOMMENDATIONS

Several possibilities come to mind for additional topics of research:

Recommendation: The hardware is sufficient to meet the next stage design goal, high speed data transfer. To accomplish this the emphasis would need to be shifted to the software to construct a program that is able to use the speed potential of the link for the data transfer.

Recommendation: A second additional major research project also suggests itself. With a minimum of hardware changes, in particular the transmitter-receiver set changed to couplers similar to the Canstar *CAF mentioned earlier, the link* could be designed for ave division multiplexed simultaneous bi-directional data transfer.

Recommendation: After the previous two recommendations were implemented, a local area network with multiple stations would meet the ultimate end goal.

LIST OF REFERENCES

1. Canstar-ADC Data Sheet, Canstar Corporation, 1987.

2. Low Cost Miniature Fiber Optic Components (Transmitters, Receivers, and Link Designs, Hewlett Packard Technical Data Sheet, February 1986.

3. Morris, David J., Pulse Code Formats For Fiber Optical Data Communication, Marcel Dekker, Inc., pp.97-110, 1983.

4. Harris Corporation, HD-15531B CMOS Programmable Manchester Encoder-Decoder Technical Specifications (Preliminary), October,1982.

5. JDR Microdevices, JDR PR-1 and PR-2 Users Manual, 1986.

BIBLIOGRAPHY

Gofton, Peter W., Mastering Serial Communications, Sybex,1986.

Harris Corporation, CMOS Digital Data Book, 1984.

Haykin, Simon, Communications Systems, John Wiley and Sons, 1983.

Irvine, Robert G., Operational Amplifier Characteristics and Application, Prentice-Hall, 1981.

Lancaster, Don, TTL Cookbook, Howard W. Sams and Co., Inc., 1974.

Motorola Inc., Linear and Interface Integrated Circuits, Series E, pp. 5-120, 1985.

Peebles, Peyton Jr., Digital Communications Systems, Prentice-Hall, Inc., 1987.

Powers, J. P., "Course Notes for Fiber Optic Systems Engineering", Navy Postgraduate School, Monterey, CA, 1987.

Sanders, Lester, "Harris CMOS Manchester Encoder-Decoder", Technical Brief 20, Harris Semiconductor Products Division.

Sanders, Lester, "HD-15530/31 Product is MIL-STD-1553A", Technical Brief 15, Harris Semiconductor Products Division.

Sanders, Lester, "Manchester II Transfers Data With Integrity, Speed", Electronic Design, March 19, 1981.

Sanders, Lester, "Using Manchester Code in Data Communication", Electronic Design Magazine, Electronic Design Conference, 1981.

INITIAL DISTRIBUTION LIST

		No. Copies
1.	Defense Technical Information Center Cameron Station Alexandria, VA 22304-6145	2
2.	Library, Code 0142 Naval Postgraduate School Monterey, CA 93943-5002	2
3.	Chairman, Code 62 Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, CA 93943-5000	4
4.	Mr. Michael Brinstool Naval Ocean Systems Command Advanced Concepts Branch San Diego, CA 92152-5000	1
5.	Sherif Michael, Code 62Mi Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, CA 93943-5000	4
6.	LCDR Robert G. Ragsdale COMCRUDESGRU TWO FPO Miami, FL 34099-4701	2
7.	J. M. Glenn, Code 62El Naval Postgraduate School Monterey, CA 93943-5000	2
8.	Harris Corporation Attn: Mr. Damien Turchin Suite 300 625 Ellis Street Mountain View, CA 94043	1